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Appl. No.: 10/736,343
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**In the United States Patent and Trademark Office**

In re the application of:
Rajendra K. Bera

Filed: 12/15/2003

For: Run-Time Parallelization of Loops in Computer Programs

Appl. No.: 10/736,343

Applicant's Docket:
JP920010326US1

Group Art Unit: 2183

Examiner: Ryan Paul Fiegle

**CERTIFICATE OF FACSIMILE TRANSMISSION**
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Anthony V.S. England — 9-28-2006
**Anthony V.S. England** — **Date**

## REMARKS RESPONSIVE TO TELEPHONE INTERVIEW

The following remarks are responsive to a telephone interview with Examiner Fiegle on September 21, 2006.

Item 1

In the interview, Examiner Fiegle questioned whether there is support in the original specification for the limitation in claim 1, for example, regarding "none of the respective numbers of pattern values exceeds three regardless of how many statements are in the loop." The following analysis is intended to more clearly explain claim 1, so that it is clear how the specification provides support for the claim language.